



*Personal Computer
Hardware Reference
Library*

**IBM Synchronous Data
Link Control (SDLC)
Communications
Adapter**

IBM SDLC Adapter



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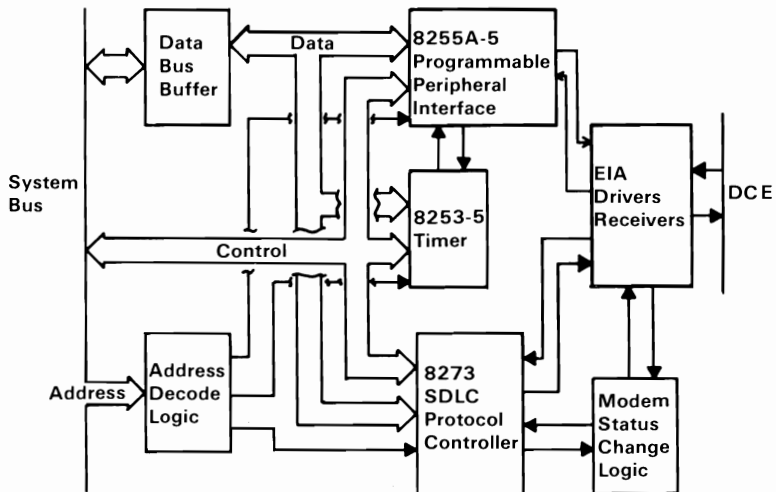
Description

The IBM Synchronous Data Link Control (SDLC) Communications Adapter provides communications support to the system in a half-duplex synchronous mode. The adapter receives address, data, and control signals from the system board through the internal bus. Electronic Industries Association (EIA) drivers and receivers connect to an RS232-C standard 25-pin, D-shell, male connector.

The adapter is programmed by communications software to operate in a half-duplex mode. Maximum transmission rate is 9600 bits per second, as generated by the attached modem or other data communications equipment.

The SDLC adapter uses an Intel 8273 SDLC Protocol Controller and an Intel 8255A-5 Programmable Peripheral Interface (PPI) for an expanded external modem interface. An Intel 8253 Programmable Interval Timer (PIT) generates timing and interrupt signals. Internal test-loop capability is provided for diagnostic purposes.

The following figure is a block diagram of the IBM SDLC Communications Adapter.



SDLC Communications Adapter Block Diagram

8273 SDLC Protocol Controller

The 8273 SDLC Protocol Controller has three operations—transmission, reception, and port read—with each operation consisting of three phases:

Command: Commands and/or requirements for the operation are issued by the system unit's microprocessor.

Execution: Executes the command, manages the data link, and may transfer data to or from memory using direct memory access (DMA), and thus freeing the system unit's microprocessor except for minimal interruptions.

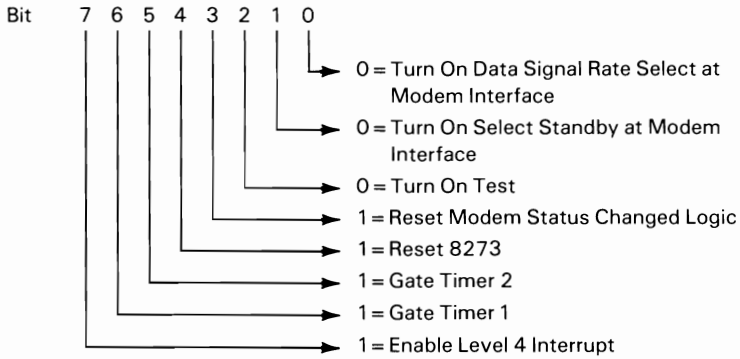
Result: Shows the effect of the command by returning the interrupt results.

Support of these phases is through the internal registers and control blocks of the controller.

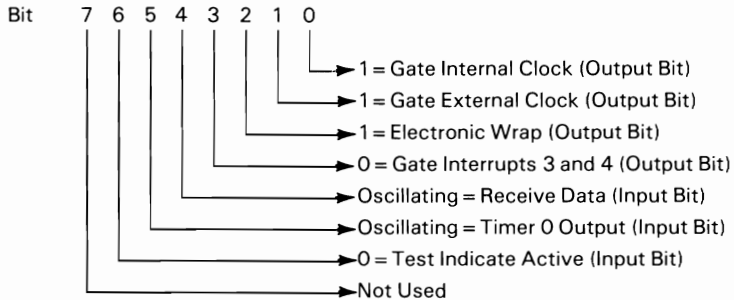
8255A-5 Programmable Peripheral Interface

The 8255A-5 PPI has three 8-bit ports—A, B, and C. Descriptions of each bit of these ports follow.

8255A-5 Port A Assignments*		Hex Address 380
Bit	7 6 5 4 3 2 1 0	
		0 = Ring Indicator is on from Interface
		0 = Data Carrier Detect is on from Interface
		Oscillating = Transmit Clock Active
		0 = Clear to Send is on from Interface
		Oscillating = Receive Clock Active
		1 = Modem Status Changed
		1 = Timer 2 Output Active
		1 = Timer 1 Output Active
*Port A is defined as an input port		

8255A-5 Port B Assignments***Hex Address 381**

*Port B is defined as an output port

8255A-5 Port C Assignments***Hex Address 382**

*Port C is defined for internal control and gating functions. It has three input and four output bits. The four output bits are defined during initialization, but only three are used.

8253-5 Programmable Interval Timer

The 8253-5 PIT is driven by a microprocessor clock signal that is divided by 2. The PIT's three counters provide the following output:

- Counter 0** Programmed to generate a square-wave signal that is used as an input to timer 2. Also connected to port C, bit 5 of the PIT.
- Counter 1** Connected to PPI port A, bit 7, and interrupt-level 4.
- Counter 2** Connected to PPI port A, bit 6, and interrupt-level 4.

Programming Considerations

Initializing the Adapter (Typical Sequence)

Before the 8273 SDLC Protocol Controller is started, the support devices on the adapter must be set to the correct modes of operation.

Setup of the 8255A-5 Programmable Peripheral Interface is accomplished by selecting the mode set address for the PPI and by writing the appropriate control word to hex 98 to set ports A, B, and C to the modes described previously in this section.

Next, a bit pattern sent to port C disallows interrupts, sets wrap mode on, and gates the external clock pins (address is hex 382, data is hex 0D). The adapter is now isolated from the communications interface.

The controller reset line is brought high through bit 4 of port B, held, then dropped. This action resets the internal registers of the controller.

8253-5 Programmable Interval Timer

The PIT's counters 1 and 2 terminal-count values are set to values that will provide the desired time delay before a level-4 interrupt is generated. These interrupts may be used to indicate to the communication programs that a predetermined amount of time has elapsed without a result interrupt (interrupt-level 3). The terminal-count values for these counters are set for any time delay the programmer requires. Counter 0 also is set to mode 3 (generates square-wave signal used to drive counter 2 input).

The counter modes are set up by selecting the address for the PIT's counter-mode register and by writing the control word for each individual counter to the device separately.

When the support devices are set to the correct modes and the 8273 SDLC Protocol Controller is reset, it is ready to be set up for the operating mode that defines the communications environment in which it will be used.

Address and Interrupt Information

The following tables provide address and interrupt information for the SDLC adapter.

Hex Code	Device	Register Name	Function
380	8255	Port A Data	Internal/External Sensing
381	8255	Port B Data	External Modem Interface
382	8255	Port C Data	Internal Control
383	8255	Mode Set	8255 Mode Initialization
384	8253	Counter 0 LSB	Square Wave Generator
384	8253	Counter 0 MSB	Square Wave Generator
385	8253	Counter 1 LSB	Inactivity Time-Outs
385	8253	Counter 1 MSB	Inactivity Time-Outs
386	8253	Counter 2 LSB	Inactivity Time-Outs
386	8253	Counter 2 MSB	Inactivity Time-Outs
387	8253	Mode Register	8253 Mode Set
388	8273	Command/Status	Out = Command In = Status
389	8273	Parameter/Result	Out = Parameter In = Status
38A	8273	Transmit INT Status	DMA/INT
38B	8273	Receive INT Status	DMA/INT
38C	8273	Data	DPC (Direct Program Control)

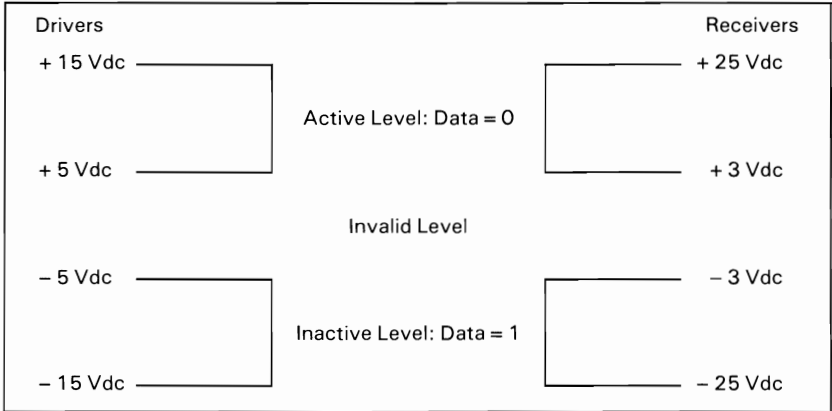
SDLC Communications Adapter Device Addresses

Interrupt Level 3	Transmit/Receive Interrupt
Interrupt Level 4	Timer 1 Interrupt
	Timer 2 Interrupt
	Clear to Send Changed
	Data Set Ready Changed
DMA Level 1 is used for Transmit and Receive	

Interrupt Information

Interface

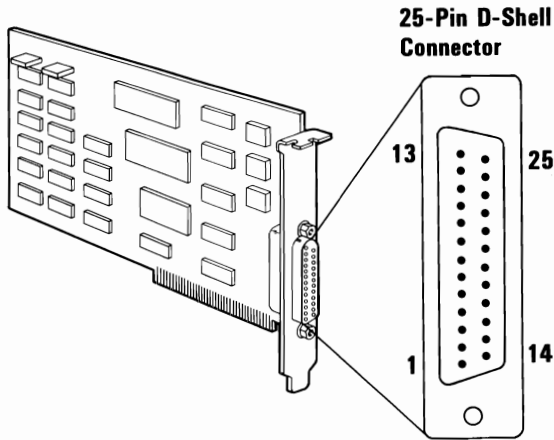
The SDLC Communications Adapter conforms to interface signal levels standardized by the Electronic Industries Association (EIA) RS232-C Standard. These levels are shown in the following figure.



Additional lines used but not standardized by the EIA are pins 11, 18, and 25. These lines are designated as 'select standby,' 'test,' and 'test indicate,' respectively. 'Select standby' supports the switched network backup facility of a modem that has this option. 'Test' and 'test indicate' support a modem-wrap function for modems that are designed for business-machine controlled modem-wraps. Two jumpers on the adapter (P1 and P2) connect 'test' and 'test indicate' to the interface.



Specifications



	Signal Name — Description	Pin	
	No Connection	1	
	Transmitted Data	2	
←	Received Data	3	
	Request to Send	4	→
←	Clear to Send	5	
	Data Set Ready	6	→
	Signal Ground	7	→
	Received Line Signal Detector	8	→
	No Connection	9	→
	No Connection	10	
←	Select Standby*	11	
	No Connection	12	
	No Connection	13	
	No Connection	14	
	Transmitter Signal Element Timing	15	→
	No Connection	16	→
	Receiver Signal Element Timing	17	→
←	Test (IBM Modems Only)*	18	
	No Connection	19	
←	Data Terminal Ready	20	
	No Connection	21	
	Ring Indicator	22	→
←	Data Signal Rate Selector	23	
	No Connection	24	
	Test Indicate (IBM Modems Only)*	25	→

External Device

Synchronous Data Link Control Communications Adapter

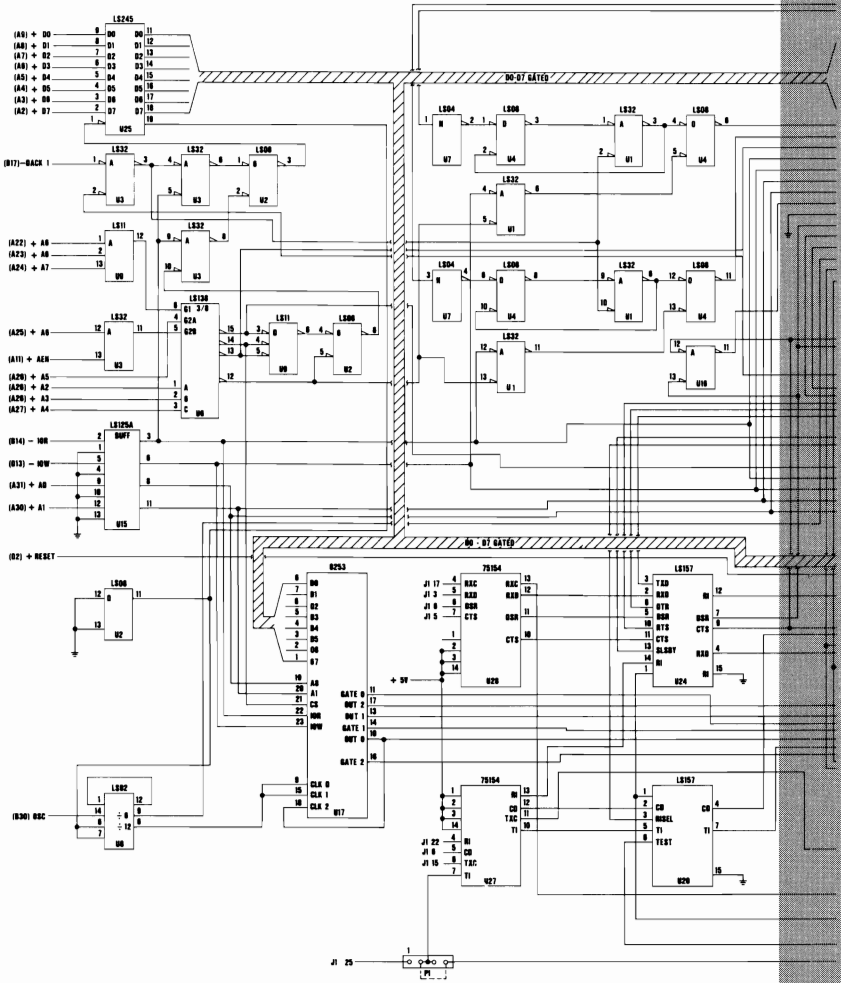
*Not standardized by EIA (Electronic Industries Association).

Connector Specifications



Logic Diagrams

The following pages contain the logic diagrams for the IBM Synchronous Data Link Control (SDLC) Adapter.



SDLC Communications Adapter (Sheet 1 of 2)

